Upgrade of Hall B Magnets' Multi-Sensor Excitation Low Voltage Chassis

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February 1, 2021

This note details the prototype upgrade—with National Instruments' single board RIO (sbRIO) controller—of the Hall B magnets' Multi-Sensor Excitation Low Voltage (MSELV) chassis implemented in the controls and monitoring system.

The cryogenic and mechanical status of the torus and solenoid—two super-conducting magnets in Hall B—are monitored closely. Cernox and PT100 sensors monitor the magnets' temperature, while load cells, strain gauges, and Hall sensors monitor the magnets' mechanical stability, e.g. structural distortions caused by gravitational, magnetic, and thermal forces [1]. The MSELV chassis' DACs and ADCs enable reading of the sensors. The DACs send to the sensors excitation voltages or currents in the range shown in Table I. Once the sensors are at the excitation voltages or currents, a voltage response proportional to the sensors' readings is generated; these voltage responses of the sensors are read by the ADCs.

Sensor	Excitation type	Excitation range
Cernox	current	0 µA–11.299 µA
PT100	current	0 mA–5 mA
Strain gauge	voltage	0 V–10 V
Load cell	voltage	0 V–10 V
Hall sensor	voltage	0 V–10 V

TABLE I. MSELV chassis sensor excitation information and ranges.

The original MSELV chassis uses a DE0-Nano FPGA board to communicate with DACs, ADCs, and an external National Instruments' compactRIO (cRIO) via RS-232. The external cRIO, called the LV cRIO, converts ADC measurements to relevant units, determines the next excitation value (if necessary), and transmits data to the control system's programmable logic controllers (PLCs). Figure 1 is a system diagram showing the original MSELV chassis' data readout communication path.

For the upgrade, the DE0-Nano FPGA board was replaced with an sbRIO, simplifying the data readout communication path to the control system's PLC, Fig. 2 [2, 3]. The sbRIO eliminates the need for the LV cRIO, which can be a potential point of failure in the communication path. Additionally, the sbRIO handles all communication to the DACs and from the ADCs, unit conversions, excitation calculations, and PLC communication.

To use the sbRIO, a program for the sbRIO's Zynq-7020 FPGA was developed to communicate with the DACs and the ADCs [4]. An additional program was developed for the sbRIO's real-time processor to communicate with the FPGA's digital communication program, to read the ADCs and set the DACs, and to convert ADC measurements to relevant units for monitoring the magnets.

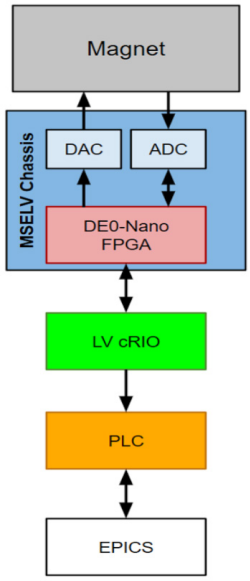


FIG. 1. System diagram of data readout for original MSELV chassis with DE0-Nano FPGA board and additional cRIO.

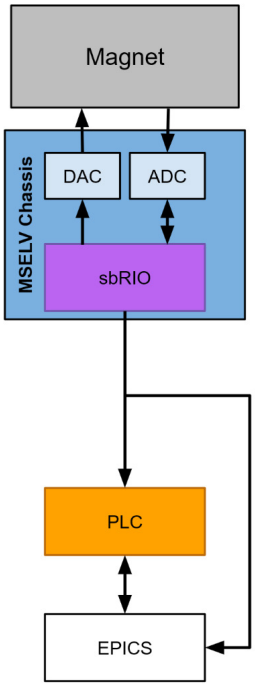


FIG. 2. System diagram of data readout for MSELV Chassis with sbRIO upgrade.

A reconfigurable input/output (RIO) mezzanine card (RMC) was designed as an interface between the sensor readout boards and the sbRIO. Figure 3 shows the system configuration and the signal paths.

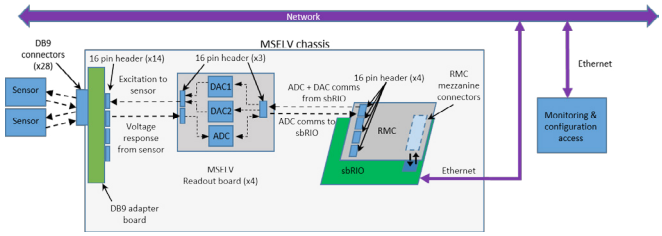


FIG. 3. System configuration and signal paths.

The top and bottom layers of the RMC, a four-layer board, are used for traces, the two inner layers for voltage and ground, Fig. 4. All layers have one ounce of copper. Minimum clearance spacing is seven mils for components and traces; via and through-hole pad clearances are 20 mils. All objects have a 25-mil clearance from board edge.

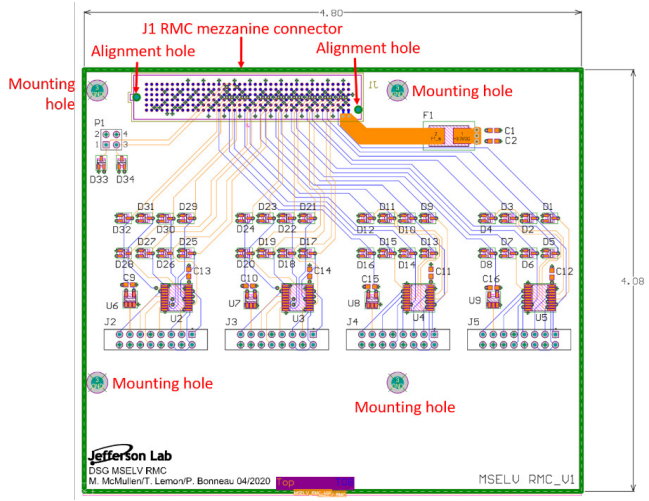
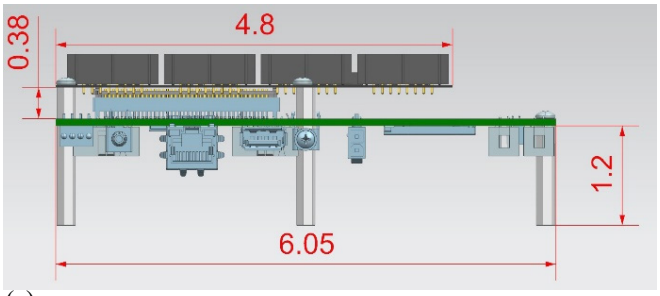


FIG. 4. RMC design. Orange traces are on the top layer, blue traces on the bottom.

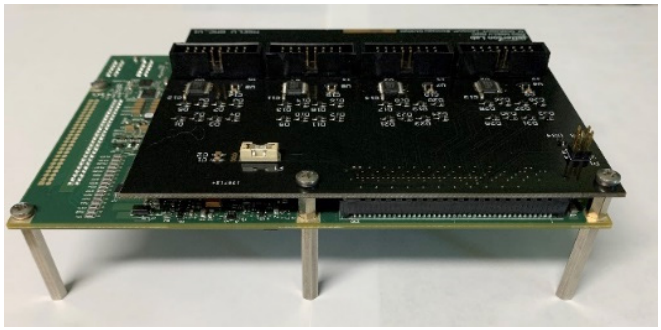
The RMC is designed to match the 55 Ω impedance of the signal sources. Connection to the sbRIO return is made by 72 pads on the Samtec SEAM-40 connector that are routed to 8-mil diameter vias connected to the RMC's ground plane. Board dimensions are 4.80" x 4.08" x 0.062".

The RMC mounts directly onto the sbRIO controller using mated mezzanine connectors, Fig. 5. To ensure proper alignment between the six rows of 40-pin contacts on the Samtec SEAM-40 connector, Fig. 6, and the solder pads on the board, the connector layout has two alignment holes, one of which is offset.

The sbRIO provides 3.3 VDC to the RMC's voltage plane via pins F39 and F40, Fig. 7. A 160-mil trace routes the voltage to the surface-mount, 750 mA fuse F1 before it terminates at the voltage plane through three 28-mil diameter vias. Two 0.1 µF capacitors (C1 and C2) decouple the voltage plane from the ground plane.



(a)



(b)

FIG. 5. (a) RMC/sbRIO interface schematic. Dimensions are in inches; (b) Photo of RMC and sbRIO interface.

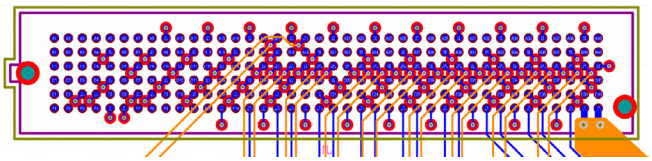


FIG. 6. Routing details of the J1 RMC mezzanine connector.

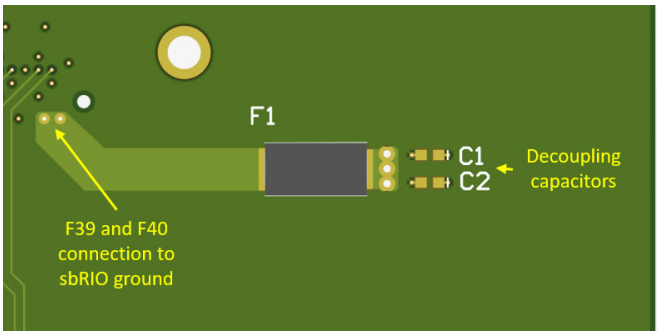


FIG. 7. Fuse F1 with decoupling capacitors C1 and C2.

Figure 8 shows the locations of four Nexperia eight-channel buffer/line drivers (U2–U5) and four Texas Instruments single-channel buffer/line drivers (U6–U9) on the RMC. Each set of drivers connects to seven output signals from the sbRIO and one input signal from the sensor readout board. The signal traces are 8-mil wide. The drivers isolate the digital communication lines and compensate for signal loss due to the wiring and cabling in the chassis.

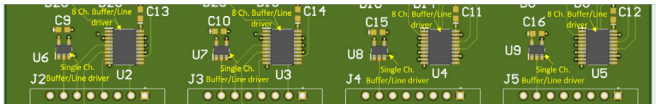


FIG. 8. Close-up view of buffer/line drivers.

Figure 9 shows—for one set of buffer/line drivers on the RMC—the signal path from the sbRIO to the sensor readout boards, on which the DACs and ADC are mounted. The top section of the schematic shows the connections for the 8-channel driver, which supports seven I/O signals from the sbRIO. Signal nets DIO_0–DIO_6 connect to driver inputs (1A1–1A4 and 2A1–2A4); the output connections (1Y1–1Y4 and 2Y1–2Y4) are shown in Fig. 9.

BRD4_DAC1_SCLK and BRD4_DAC2_SCLK are the serial clocks inputs to the DACs. DAC synchronization is provided by BRD4_DAC_SYNC. Two inputs to the DACs and one input to the ADC of the connected readout board are provided by BRD4_DAC1_DIN, BRD4_DAC2_DIN, and BRD4_ADC_DIN. The last two connections to the sensor boards are chip select BRD4_ADC_CS and serial clock BRD4_ADC_SCLK for the ADC.

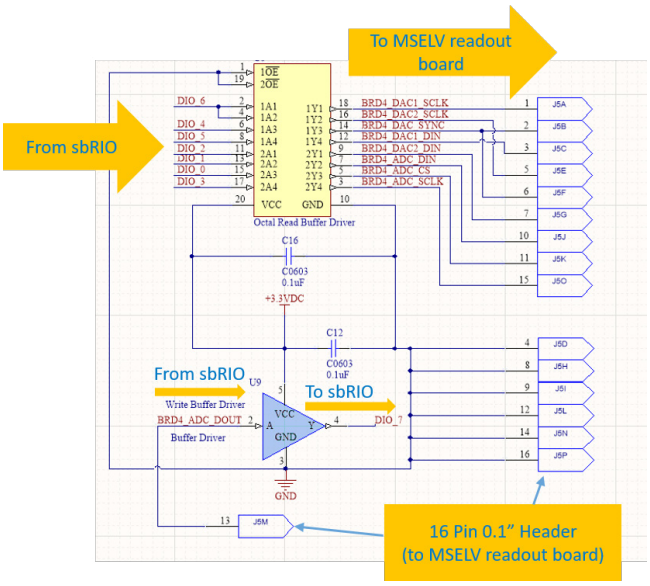


FIG. 9. Data path for a set of buffer/line drivers. Each set has one 8-channel (for the output signals) and one single-channel driver (for the input signal).

In the lower section of the diagram, ADC output signal net BRD4_ADC_OUT is connected from the sensor readout boards to the sbRIO. The signal connects to the input of the single-channel buffer/line driver A, which sends the ADC data to the sbRIO from the driver output Y via net DIO_7. Table II summarizes the number of DACs, ADCs, and communication lines on the RMC.

Figure 10 shows four sets of eight Schottky diodes, which protect each digital input/output channel by preventing reverse current flow into a channel in case there is a short on the RMC or on the sensor readout board. Each signal trace is terminated at the input of a reverse-biased Schottky diode, before it connects to the buffer driver input. Such a termination limits the amplitude of signal reflections

The four 16-pin, input/output headers J2–J5 connect the RMC to the DAC boards. The 4-position jumper P1 is used for loop-back signal testing and is located in the upper left section of the RMC.

	Property	Per read-out board	Chassis total
DACs	component quantity	2	8
	sbRIO-to-DAC communication lines	4	16
ADCs	component quantity	1	4
	sbRIO-to-ADC communication lines	3	12
	ADC-to-sbRIO communication lines	1	4
	total ADC communication lines	4	16
RMC totals	sbRIO-to-component (output) communication lines	7	28
	component-to-sbRIO (input) communication lines	1	4
	total communication lines	8	32

TABLE II. Communication lines needed for each component in the MSELV chassis.

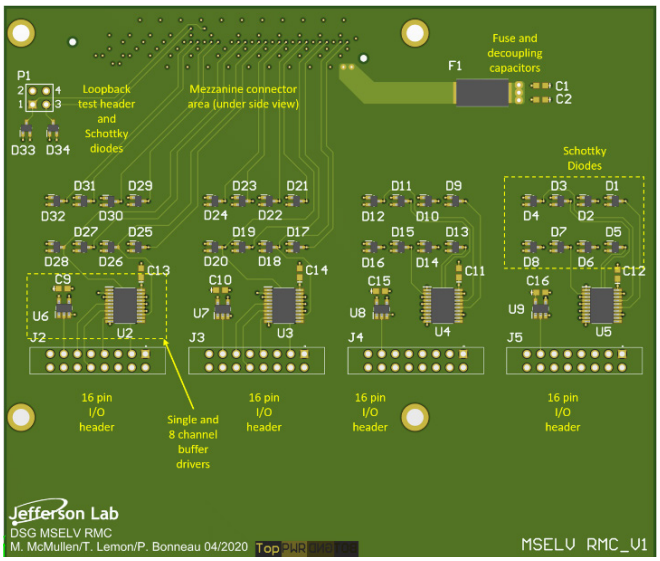


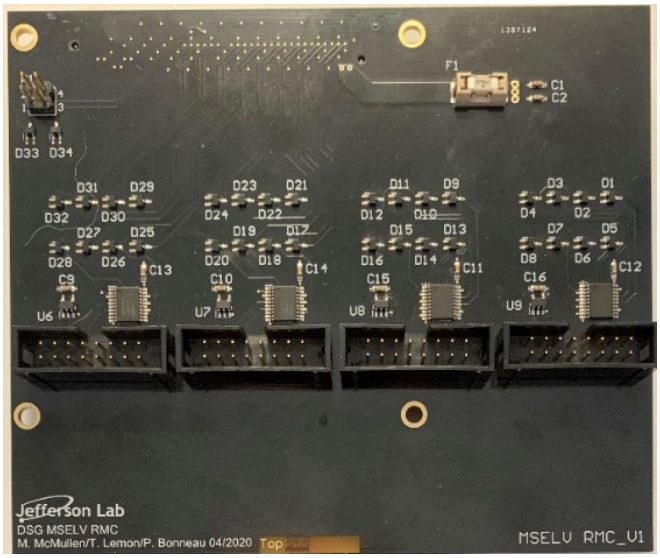
FIG. 10. Rendering of the RMC with key features.

Figure 11 shows photographs of the top and bottom sides of a populated RMC board.

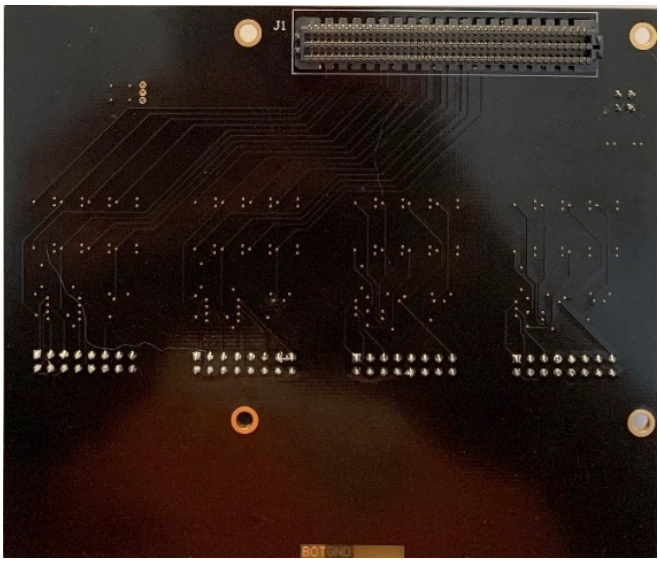
During initial testing, all eight DAC outputs to the chassis' rear sensor ports were read. However, none of the four ADCs in the chassis could be read.

Inspection of the label on the single-channel buffer/line driver showed that the driver selected did not match the one used on the board being replaced, though it matched the original schematic—this was because the part number in the schematic had not been updated.

The initially selected single-channel driver was SN74LVC1G07, which, if its input pin is held high makes the output pin enter a high-impedance state, or tri-state,



(a)



(b)

FIG. 11. (a) Photo of RMC top. (b) Photo of RMC bottom.

rather than passing through the high input signal, eliminating all digital communication signals. When the correct driver SN74LVC1G17 was used, the ADCs responded as expected, passing through the high input signal to its output pin. A summary of the single-channel driver behavior is noted in Table III.

The RMC was re-tested; and functioned correctly. All DACs and all ADCs in the MSELV chassis were set and read.

In summary, a new version of the MSELV chassis based on a National Instruments' sbRIO was developed. This version of the MSELV removes a potential point of failure from the sensor readout path.

For the sbRIO to be integrated into the MSELV chassis, an RMC was designed, fabricated, populated, tested, and debugged. The RMC and sbRIO were installed in the MSELV chassis, tested, and debugged, completing the successful sbRIO upgrade of the MSELV chassis.

Buffer driver part #	Chip output when input is low	Chip output when input is high
SN74LVC1G07 incorrect	low	high impedance
SN74LVC1G17 correct	low	high

TABLE III. Summary of single-channel buffer/line driver responses with high and low inputs.

[1] T. Lemon, et al., *Analysis of Hall B Solenoid Load Cells' Readings During Fast Dumps*, DSG Note 2019-02, 2019.
[2] P. Bonneau, et al., *FPGA Upgrade Proposals for the Hall B Torus and Solenoid Control and Monitoring Systems*, DSG Note 2019-37, 2019.
[3] T. Lemon, et al., *sbRIO-based Multi-Sensor Excitation Low Voltage Chassis for Hall B Magnets*, DSG Note 2019-43, 2019.
[4] T. Lemon, et al., *sbRIO-based Multi-Sensor Excitation Low Voltage Chassis for Hall B Magnets sbRIO Digital Communication Within the Multi-sensor Excitation Low Voltage Chassis*, DSG Note 2020-01, 2020.