

Thermal Analysis of sbRIO-9629 to be Used in the Hall B RICH II Hardware Interlock System

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RICH II's hardware interlock system uses a National Instruments sbRIO-9629 controller. The design of the system's hardware must ensure that the CPU and the FPGA remain below their operating temperature limits. This note discusses the Ansys software [1] simulation, which shows that when the sbRIO and associated components are installed in a 2-mm-thick aluminum chassis with a heat spreader configured to provide a thermal conductive path to the chassis, the maximum temperature on the sbRIO will be $\sim 60^\circ\text{C}$.

Heat generated in sbRIO chassis must be removed to ensure that the operating temperature limits of the CPU and the FPGA, the two main heat sources, are not exceeded, Table I.

Item	Item details	Max. heat generated [W]	Temperature limit [$^\circ\text{C}$]
CPU	Intel Atom E3845 Quad-Core 1.91 GHz processor	10	98
FPGA	Xilinx Artix-7 XC7A200T	10	110

TABLE I. sbRIO heat-generating components.

For the Ansys simulation, an NX12 model of a 2-mm-thick-aluminum-panel chassis was generated, Fig. 1. In the chassis, the sbRIO populated with the CPU and the FPGA, the heat spreader—spreads the generated heat and conducts it to the chassis—and a thermal pad—made of silicon material to improve contact of the sbRIO and its components with the heat spreader—were installed, Figs. 1 and 2.

The simulation used an ambient temperature of 22°C and a convection film coefficient of $5 \times 10^{-6} \text{ W}/(\text{mm}^2\text{C})$, imported from Ansys's *Stagnant Air – Simplified Case* convection model. Both FPGA and CPU were considered to generate 10 W.

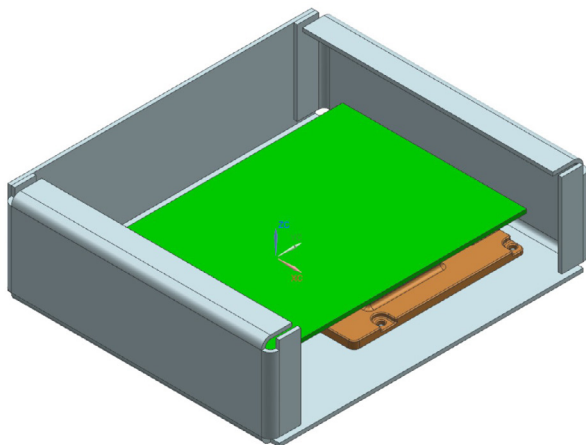


FIG. 1. NX12 model of sbRIO (green) and heat spreader (brown) in chassis (grey). The thermal pad cannot be seen. Front and top panels are removed to show sbRIO.

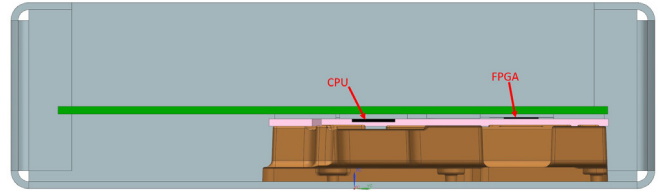


FIG. 2. Side view of NX12 model. sbRIO (green) and heat spreader (brown) in chassis (grey). The thermal pad (pink) improves contact of the sbRIO and its components with the heat spreader.

Analysis result showed that the maximum steady state temperature was $\sim 60^\circ\text{C}$, Figs. 3 and 4.

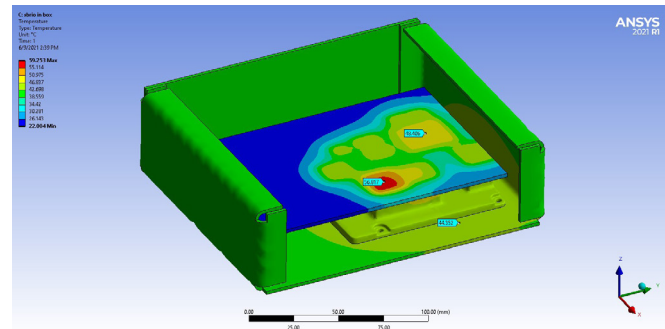


FIG. 3. Ansys analysis results of sbRIO in chassis. In figure, front and top panels are removed to show sbRIO.

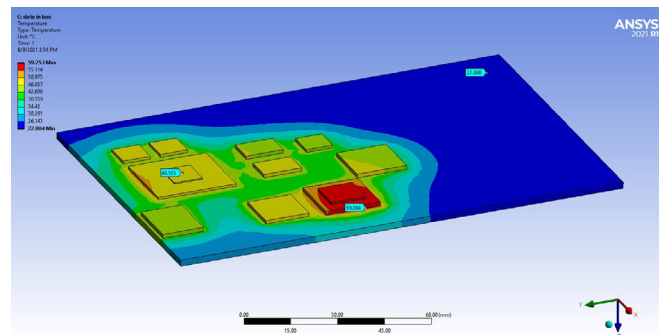


FIG. 4. Ansys thermal analysis results of only the sbRIO. In figure, chassis and other components are hidden. Thermal probes in blue are placed on the FPGA (red) and on the CPU.

In summary, Ansys analysis confirms that the designed configuration works.

[1] Ansys, Inc., *Ansys Mechanical Overview*, 2020.