

# Selection of Parts for the Reconfigurable Input/Output Mezzanine Card of the Hardware Interlock System for Hall B's Second Ring Imaging Cherenkov Detector

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This note discusses how the parts selected for the reconfigurable input/output mezzanine card (RMC) facilitate its designed functions.

The RMC [1] for the hardware interlock system of the second ring imaging Cherenkov (RICH) detector is designed to buffer and minimize the transmission loss of the I<sup>2</sup>C signals between the sbRIO and the SHT35 sensors located in the detector, and to control the solid state relays that interlock the CAEN power supply.

Each I<sup>2</sup>C communication line on the RMC has two sets of Schottky diodes (BAT54SDW from DIODES Incorporated [2]), D13 and D14 in Fig. 1—one for the sbRIO digital input/output channel and the communication connection of the buffer driver controller, the other for the buffered output. These Schottky diodes were selected because they allow digital signals in the range of 0–3 V to pass through and because of their low forward voltage drop of ~0.5 V.

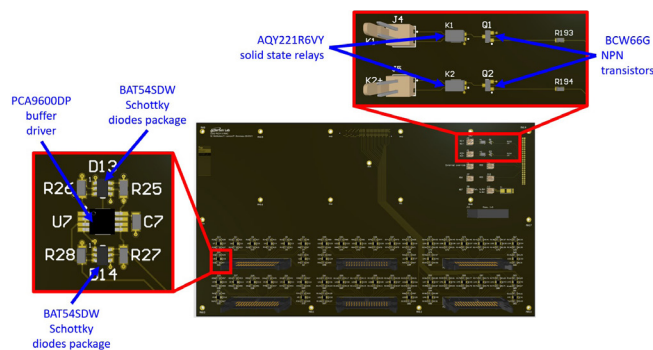


FIG. 1. Altium rendering of RMC, with two details.

The buffer driver (PCA9600DP from NXP Semiconductors [3]) was selected for the buffering circuit, Fig. 2, to minimize transmission loss of the I<sup>2</sup>C signals over ~100-ft CAT7 Ethernet cables, between the sbRIO's digital outputs and the SHT35 sensors [4].

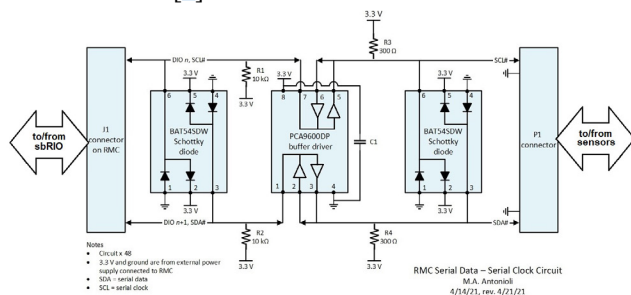


FIG. 2. RMC schematic. sbRIO connects at J1. Circuit is repeated 48 times on RMC to monitor the 24 SHT35 sensor boards (a total of 48 sensors).

The sbRIO sends the clock and data signals to the PCA9600DP buffer driver, which outputs the signals with a delay of less than 100 ns. In contrast to the 24-mA drive capability of the sbRIO [5], the buffer driver has a 60-mA drive capability, which minimizes transmission loss of the signal.

An RMC communication line with the Schottky diodes is shown in Fig. 3. Multisim Live, an online SPICE simulator from National Instruments, was used to simulate the voltage that would be seen by the sbRIO or the buffer driver if the voltage on the communication line jumped to 24 V.

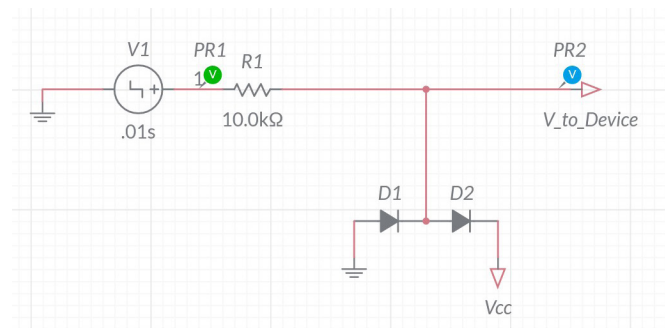


FIG. 3. Schematic used in Multisim Live. Input to Schottky diode circuit (modeled as a 50-VDC step function after a 10-ms delay) was measured at the green probe *PR1*. The voltage seen by the device was measured at the blue probe *PR2*.

In Fig. 4, *PR1* and *PR2* show the voltage over time measured by Multisim Live. With the Schottky diodes, voltage measured at *PR2* is 3.54 V.

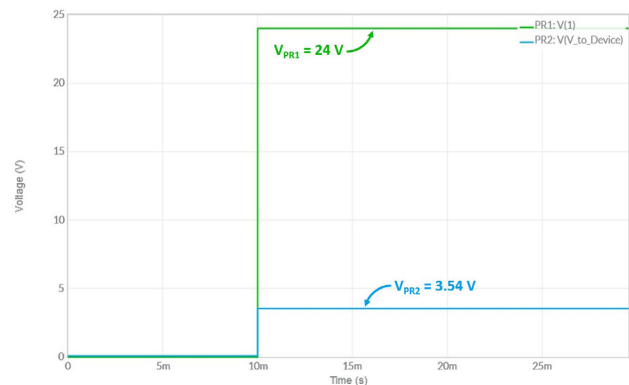


FIG. 4. Green trace is the voltage measured by *PR1*, blue trace voltage measured by *PR2*.

Figure 5 shows the circuit that facilitates the sbRIO's control of the solid state relays K1 and K2 (AQY221R6VY from Panasonic [6]) to interlock the CAEN power supply. The two NPN transistor switch circuits provide 3.3 VDC from the hardware interlock chassis' 3.3-VDC, 9-W power supply to the two solid state relays. The NPN transistor switch circuits are controlled from the two analog outputs on the sbRIO's multiple-input-output connector. The circuit provides the 50 mA required to drive the solid state relays, higher than the  $\pm 3$  mA of the sbRIOs' analog outputs.

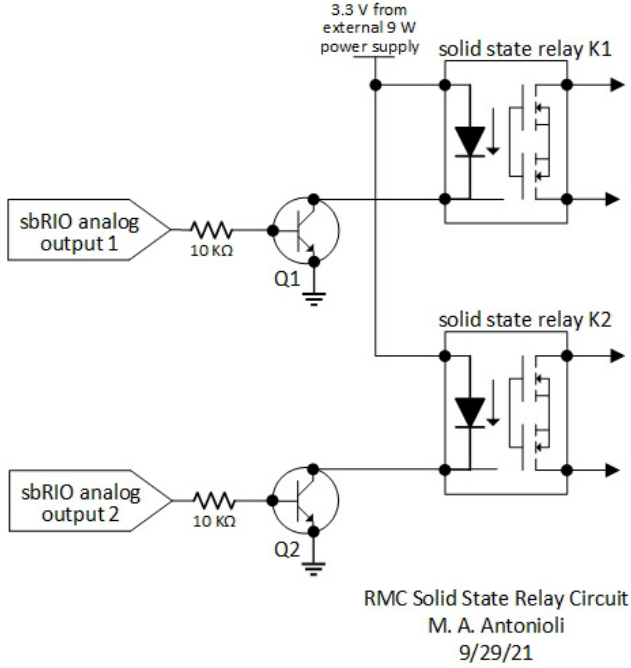


FIG. 5. Solid state relays control circuit.

NPN transistors (BCW66G from nexperia [7]) Q1 and Q2 were selected for their 1.25-V base saturation voltage that both the sbRIO's analog outputs and the sbRIO's 3.3-V digital outputs can provide.

In summary, the aforementioned RMC parts were selected to buffer and to minimize the transmission loss of the I<sup>2</sup>C signals between the sbRIO and the SHT35 sensors, and to control the solid state relays that interlock the CAEN power supply. Bench tests and simulations validate the selected RMC parts.

- [1] [Marc McMullen, et al., \*Design of the Reconfigurable Input/Output Mezzanine Card for the Hardware Interlock System of Hall B's Second Ring Imaging Cherenkov Detector\*, DSG Note 2021-22, 2021.](#)
- [2] [Diodes Incorporated, \*Surface Mount Schottky Barrier Diode Arrays\*, 6/2016.](#)
- [3] [NXP Semiconductors, \*PCA9600 Dual Bidirectional Bus Buffer – Rev. 6\*, 9/2015.](#)
- [4] [Marc McMullen, et al., \*Sensirion SHT-35 Sensor Board Design for Hall B's RICH II Detector\*, DSG Note 2021-14, 2021.](#)
- [5] [National Instruments, \*sbRIO-9629 Single-Board RIO Controller Specifications\*, January 8, 2021.](#)
- [6] [Panasonic, \*SSOP 1 Form A Solid State Relay Data Sheet\*, 2019.](#)
- [7] [Nexperia, \*BCW66 series 45 V, 800 mA NPN General-Purpose Transistor\*, April 21, 2017.](#)